ONE-TRANSISTOR FLOATING-BODY DRAM CELL IN BULK CMOS PROCESS WITH ELECTRICALLY ISOLATED CHARGE STORAGE REGION

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ABSTRACT

A one-transistor, floating-body (1T/FB) dynamic random access memory (DRAM) cell is provided that includes a field-effect transistor fabricated using a process compatible with a standard CMOS process. The field-effect transistor includes a source region and a drain region of a first conductivity type and a floating body region of a second conductivity type, opposite the first conductivity type, located between the source region and the drain region. A buried region of the first conductivity type is located under the source region, drain region and floating body region. The buried region helps to form a depletion region, which is located between the buried region and the source region, the drain region and the floating body region. The floating body region is thereby isolated by the depletion region. A bias voltage can be applied to the buried region, thereby controlling leakage currents in the 1T/FB DRAM cell.